2 Introduction to Transport in Silicon-Germanium

With low power dissipation, high integration levels, good noise immunity, high cost-effectiveness and reliability, silicon CMOS (Complementary Metal-Oxide-Semiconductor, see Chapter 7) technology occupies a dominant position in microelectronics. However, the low mobilities* of electrons and holes in silicon limits its application to relatively low frequencies, leaving III-V materials such as Gallium Arsenide (and related materials) to fulfil roles in mobile communications and the like.[1,2,3]

Strained layers of silicon and silicon-germanium alloy offer scope for dramatic improvements in mobility, and therefore performance. New technology may possibly be incorporated into standard silicon CMOS processing, making the transition favourable to industry.[1,2,3]

Room temperature mobilities in silicon MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistor) tend to be around $300\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for electrons, and less than $100\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for holes, for sheet densities of the order of 10^{13}cm^{-2}.[1] The advantage of CMOS microelectronics is its very low power consumption (which facilitates higher packing densities) compared to bipolar or NMOS technologies: ideally, a CMOS circuit only dissipates power as it is switching state and it is therefore desirable to equalize the switching time of n and p channel devices, and minimize the switching time overall. In practice this currently means that p-channel MOSFETs in CMOS integrated circuits must be made wider than corresponding n-channel MOSFETs for their conductances to match, and there is a trade-off between channel width and packing density.

It would be advantageous to match the mobilities of electrons and holes, and to increase the mobilities of both electrons and holes overall. This will facilitate higher

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* Mobility is a figure of merit for semiconductor materials and is defined and explained in Chapters 3 and 4. The conductivity of a device is proportional to the product of the density of charge carrying particles (number per unit area of material) and their mobility, but the maximum frequency at which a MOSFET can be operated is related to the minimum transit time of carriers through the device and therefore to the mobility of the carriers.[3]

packing densities, higher operational frequencies or lower-power operation, depending on the requirements of the application.

In addition to this desire to contribute directly to the semiconductor industry, silicon-germanium alloy strained-layer systems can be studied from the perspective of the fundamental physics of semiconductors. The results of these studies (often at liquid-helium temperatures or employing large magnetic fields, on devices with relatively poor characteristics) can then be considered when optimizing the design of industry-level devices for room-temperature operation.

In the field of silicon-germanium research, the highest mobilities have been observed in systems with relatively low sheet carrier densities, meaning that the overall conductivity of the system is not necessarily impressive.[4,5,6] The relationship between mobility and carrier density is fundamental to characterizing the mechanisms which limit the mobility and will be explored throughout this thesis, especially in the realm of higher sheet densities of both electrons (Chapter 6) and holes (Chapter 5). This should lead, in conjuction with respectable mobilities, to the production of high conductivity devices with potential for high frequency operation.[7] Additionally, research is traditionally carried out on devices which may be up to the order of a millimetre in length and measured parameters may or may not scale down to integration-scale devices on the scale of a few microns in length. A device of this scale will be investigated in Chapter 5. Regarding a new approach to integrating and balancing electron and hole channels, a device which features both will be investigated in Chapter 7.

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