7 Coupled Channel Devices

7.1 Abstract

Chapters 5 and 6 explored the transport properties of holes and electrons respectively in silicon-germanium heterostructures. In this chapter, devices are presented in which electron and hole gases can both be induced by suitable gate bias conditions. The electron gas is formed in an inversion layer at the interface between silicon and silicon dioxide in the conventional n-channel MOSFET manner; the hole gas is formed by inverted modulation doping of a quantum well of pseudomorphically-grown $Si_{0.8}Ge_{0.2}$ alloy.

The heterointerface at which the hole gas forms is either approximately 100nm (on wafer 50/51) or 40nm (on wafer 50/53) away from the oxide interface at which the electron gas forms. The electron and hole systems are contacted separately by sets of n^+ and p^+ contacts, the former being implanted to a depth of around 25nm and the latter essentially reaching down through the whole heterostructure.

These devices were initially conceived and designed to explore the novel transport phenomena which interactions between co-existing electron and hole gases in silicon-germanium may invoke. The discussion will show that the structures investigated can not support co-existing electron and hole gases, and alternative designs will be presented.

7.2 Introduction

There are two contrasting aims behind attempts to create a semiconductor structure that features spatially separated, interacting, 2-dimensional charge carrier gases. There is the desire to study the fundamental interaction between carriers, in order to develop a better understanding of the physics of semiconductor materials. Then, there is also the desire to create a device with operation analogous to a CMOS integrated circuit, but with p-type and n-type channels arranged vertically rather than laterally.

7.2.1 Interactions

Lozovik and Yudson suggest a new mechanism of superconductivity based on the pairing of spatially separated electrons and holes due to their Coulombic attraction.[1] Their calculations indicate that the critical temperature may be as high as a few hundred Kelvin for reasonably realistic experimental parameters. This possibility has been considered in more detail since then.[2,3,4,5] Thakur, Neilson and Das estimate that the superconducting transition temperature for experimentally accessible carrier densities and layer separations is 100mK.[5]

Electrons and holes, when they are both present in a semiconductor, can pair up by way of their Coulombic attraction. A bound electron-hole pair (an exciton) is boson-like, since electrons and holes are both fermions. In analogy with Cooper pairs in a superconductor (boson-like pairs of electrons, bound together by phonons) a collection of excitons is expected to undergo Bose-Einstein condensation under appropriate conditions.[4] One of these conditions is that the recombination lifetime of the electron-hole pair is longer than the thermal energy relaxation time (see Equation 6.30) so that the condensed state can form and be observed, usually by photoluminescence.[6,7] In indirect-gap semiconductors, such as bulk silicon and germanium, the recombination lifetime satisfies this condition but it has been established that the exciton condensate can not exist due to competition with a more stable electron-hole plasma droplet phase.[4]

Heterostructures provide a method of extending the recombination lifetime: by suitably arranging the materials of the structure (and if necessary applying an appropriate electric field) the valence and conduction bands can be bent into a profile which localizes electrons and holes seperately in their own quantum wells, as shown in Figure 7.1. Coulombic interaction can still lead to the formation of bound electron-hole pairs but, provided the potential barrier between the carrier gases is high and/or wide enough to prevent significant tunnelling, recombination is prevented.

Figure 7.1 Proposed band profile of coupled-channel devices.[21] Electron and hole gases co-exist within ~100nm of each other.

Experimental work on interacting, spatially separated carrier gases has been performed using GaAs/AlGaAs heterostructures, using photoluminescence techniques to directly probe for the presence of excitons.[6,7] However, the transport properties of the interacting electron-hole layers are of the most interest and there is experimental work of this nature on GaAs/AlGaAs[8,9] and InAs/GaSb/AlSb[10] structures (interesting because the conduction band of InAs falls at a lower energy than the valence band edge in GaSb) but not Si/SiGe. These structures must be designed so that independent electrical contact to the electron and hole gases can be made.

7.2.2 Vertical CMOS

A device which features vertically separated 2-dimensional electron and hole gases, where their carrier densities can be modulated, presents itself as an alternative to the standard CMOS architecture which features modulated electron and hole gases arranged laterally as MOSFETs as part of a silicon integrated circuit.[11,12] The use of silicon-germanium technology within conventional CMOS architecture would seem to require complicated heterostructure design in any case (if the full benefits of compressively strained germanium rich layers for p-channel conduction and tensile-strained pure silicon for n-channel conduction are to be reaped)[13,14,15,16,17,18] so it is worth investigating the possibility that novel design may find additional benefits to silicon-germanium CMOS technology.

An inverter is shown in Figure 7.2, in terms of circuit schematics, conventional CMOS structure and proposed vertical CMOS structure. In this case, interaction between the two carrier gases is not desired but this is unlikely to be a problem for a device working at room temperature. As the band profiles in Figure 7.3 show, suitable gate bias causes either an electron gas or a hole gas to form, but the two gases do not co-exist as in Figure 7.1.

Figure 7.2 Conventional CMOS versus vertical CMOS: the case for a simple inverter is shown, with the circuit schematic at the top right. In the case of familiar conventional CMOS, the p-channel and n-channel devices sit side by side and the conducting channels are formed at the interface between the silicon and the oxide.[12] In the case of vertical CMOS, a positive gate bias forms an n-channel at the oxide interface and a negative gate bias forms a p-channel at the upper heterointerface, as the band profiles in Figure 7.3 show.

Figure 7.3 Proposed band profiles of a vertical CMOS device. The substrate (here shown to be slightly positively doped) is to the right, and the left edge of the profile is the silicon-silicon dioxide interface. Negative gate bias (upper profile) forms a hole gas at the top of the $Si_{1-x}Ge_x$ alloy and positive gate bias (lower profile) forms an electron gas at the oxide interface. The gases do not co-exist, as in Figure 7.1. If the gate bias in the upper panel becomes slightly more negative, then the valence band will reach the Fermi level and a hole gas will form at the oxide interface.

7.3 Structure and Fabrication

The heterostructure and device design and processing work was completed by Dr. C. J. Emeleus, in conjunction with Dr. M. A. Sadeghzadeh.[19]

The heterostructures, described by Figure 7.4, were grown by MBE on three 4" silicon n^- 8-12Ωcm substrates. 300nm of intrinsic silicon (at 830°C) was followed by 40nm of silicon (at 500°C) doped with boron to a concentration of 2×10^{18}cm^{-3} giving an integrated dose of 8×10^{12}cm^{-2}. A 34nm intrinsic spacer layer was then grown (at 500°C) followed by 15nm of $Si_{0.8}Ge_{0.2}$ alloy at 650°C. This is double the equilibrium critical thickness of this alloy concentration but well below the metastable thickness for this growth temperature.[20] The intrinsic cap layer was either 90nm (for wafers 50/51 and 50/52) or 30nm (for wafer 50/53).

The 2-dimensional hole gas (2DHG) areas were defined at this point by etching this heterostructure away between devices on each chip, and the wafers were subject to an RCA clean which grows 1 or 2 nm of oxide.

A 9 or 10nm native oxide was further grown on wafers 50/51 and 50/53, consuming 4 or 5nm of the cap layer. 300±50nm of “low temperature” oxide (LTO) was then deposited using a CVD gas-flow technique at Southampton University. The native oxide should provide a better silicon-oxide interface compared to that formed when LTO is deposited directly onto silicon. However, the native oxide process required one hour at 720°C which may cause some relaxation of the strain in the alloy layer or diffusion of boron dopant atoms. The relative performance of 50/51 and 50/52 should make this clear.

Shallow n^+ contacts were made using low energy (10keV) implantation of arsenic ions before the native oxide was grown, in a process developed by Dr. C. P. Parry.[21] Deep p^+ contacts were made using 70keV implantation of BF_2^+ through the native oxide, before the LTO deposition process.

Figure 7.4 The heterostructure as grown on wafer 50/51. 50/52 and 50/53 differ in the manner shown.

Simulations (using the TRIM program of J. F. Zeigler and J. P. Biersack)[22] confirm that the n^+ implantations reach a depth of 20nm, and the p^+ implantations reach a depth of over 200nm, well beyond the Boron doping layer. Windows were patterned through the oxide and Ti+Al/Si metal contacts were made.

Most of the devices are Hall bars, many with gates and full sets of n^+ and p^+ contacts as shown in Figure 7.5. The aim of the design was to realize the band profile shown in Figure 7.1.[21] Two cap layer thicknesses are available: devices on wafer 50/53 with its smaller cap thickness of 30nm should be more likely to show interaction effects than devices on wafer 50/51 or 50/52, but are also more likely to suffer from possible problems caused by the shallow n^+ contacts reaching the 2DHG.

Expected Electronic Properties

An estimate of the expected sheet density can be found by considering Figure 3.1 and Equation 3.1. If E_0 and E_A are ignored and the field created by the sheet of carriers is equated with the field required to change the potential by the heterojunction valence band offset ΔE_V over the length d:

$$\frac{p_S q}{\epsilon_0 \epsilon_{Si}} = \frac{\Delta E_V}{d} \qquad 7.1$$

Assuming an offset value of 140meV for $Si_{0.8}Ge_{0.2}$[23] results in an expected sheet density of $3 \times 10^{11} cm^{-2}$ as designed by Dr. M. A. Sadeghzadeh using a self-consistent Poisson-Schrödinger calculation.[19,21,24,25]

Applying a positive bias to the gate should produce an inversion layer of electrons at the silicon/silicon dioxide interface and form a band profile as in Figure 7.1. A key feature is that the p^+ implants should exclusively contact the 2DHG in the alloy, and the n^+ implants the 2DEG inversion layer. Each system of n^+ or p^+ contacts and gating should form a MOSFET-like device and this should be readily visible in room-temperature IV characterization.

Figure 7.5 The pattern of a double Hall bar, a typical device. Metal (for contact pads and the gate) is shown in blue. Black areas are windows through the oxide. Red areas show the extent of the heterostructure (Figure 7.4) itself. Shallow n^+ implants are green, deep p^+ implants are pink. The Hall bar itself is 20µm wide.

7.4 Results of IV Characterization

The simplest way of characterizing the structures was to connect suitable gated Hall bar devices in a MOSFET configuration at room temperature. Contacts at either end of the bar were designated (arbitrarily) as source and drain, and voltages were measured relative to the source. The shallow contacts are expected to contact to the inversion layer induced by application of a suitable gate voltage, in exactly the way an n-channel MOSFET operates.

7.4.1 Basic 2-Terminal Characterization at 300 K

Shallow Contact Results

Figure 7.6 shows the drain current characteristics of a gated Hall bar from wafer 50/51. The drain-source voltage, V_{DS}, was applied along the Hall bar via n^+ contacts, so the drain current I_D should be being passed through the device mainly by electrons in an inversion layer at the silicon/silicon-dioxide interface. The characteristics are similar to those of an n-type MOSFET: As the gate voltage is made more positive, the drain current increases. The gradient (that is, the conductivity) of the curves in Figure 7.6 changes when V_{DS} is approximately 0.5V. However, as V_{DS} continues to increase to over 1.0V, it can be seen that drain current increases for all gate voltages. This is similar to punch-through, which arises in short-channel MOSFETs when the depletion layer created by large V_{DS} extends all the way from the drain to the source.[12] However, the effect seen here is unlikely to be related directly to punch-through since the Hall bar is 160μm long, over a hundred times longer than the channel of a “short channel” MOSFET.[12]

Figure 7.6 Drain current characteristics of a gated Hall bar on wafer 50/51, as measured using shallow n^+ contacts. Characteristics are similar to those of an n-type MOSFET.

Figure 7.7 shows that the drain current has a clear threshold voltage (V_{TS}=15V) at which $I_D \propto (V_{GS} - V_{TS})^2$. The gradient of the I_D vs. V_{GS} lines (the transconductance) becomes smaller again as V_{GS} increases further and the channel saturates. No significant current flows for gate bias values between zero and -100V. (These gate voltages are two orders of magnitude greater than those for typical MOSFET device operation since the gate oxide is very thick.)

Deep Contact Results

Figure 7.8 and Figure 7.9 should be compared to Figure 7.6 and Figure 7.7 respectively. Figure 7.8 shows that the (2-terminal) resistance as measured between deep p^+ contacts depends very little on the magnitude of V_{DS} but is influenced by the gate voltage V_{GS}. This can be seen more clearly in Figure 7.9. At positive gate voltages, there is very little variation of I_D with V_{GS}, for a given drain-source voltage but as V_{GS} becomes more negative, I_D increases. Figure 7.7 shows that no current flows between the shallow n^+ contacts for gate voltages smaller than 15V, provided V_{DS} is below 1.0V. It does not seem to be possible to prevent conduction between the deep contacts with suitable gate bias, so either it is impossible to turn the p-channel off or there is conduction through the boron doping layer at all times.

Interpretation of Room Temperature Results

The n-type MOSFET-like behaviour seen in the shallow contact characterization implies that at gate voltages more positive than 15V an inversion layer forms at the silicon/silicon dioxide interface. If there was some way in which the shallow contacts were providing a current path through the hole gas (which is presumably buried deep in the structure) then there would be no way of preventing drain current flow through the shallow contacts with gate bias: if the deep contacts are contacting the hole gas then Figure 7.9 shows that the hole gas is never depleted to the extent that it does not conduct. This implies that the shallow contacts do indeed only contact to the electron inversion layer for V_{DS} smaller than 1.0V.

Figure 7.7 Transfer characteristics of a gated Hall bar, as measured using shallow n^+ contacts. Characteristics are similar to those of an n-type MOSFET.

Figure 7.8 Drain current characteristics of a gated Hall bar, as measured using deep p^+ contacts. Characteristics bear little resemblance to those of a p-type MOSFET.

Figure 7.9 Transfer characteristics of a gated Hall bar, as measured using deep p^+ contacts, following on from Figure 7.8.

However, as the drain-source voltage across the shallow contacts is increased it can be seen that drain current flows even for sub-threshold gate voltages. Since it is unlikely that there is a direct path between shallow contacts (which are very far apart by usual MOSFET standards) then it is probable that the current is somehow passing through the hole gas. The non-zero V_{DS} needed to invoke this conduction path implies that there is some kind of barrier, probably a depletion zone, between the shallow contacts and the hole gas.

All the above results are from wafer 50/51. By contrast, devices on wafer 50/52 showed very little increase in drain current between p^+ contacts as gate bias was made more negative. This may suggest that the increase seen in Figure 7.9 is due to the formation of a hole gas at the oxide interface; the difference in quality of this interface between 50/51 and 50/52, due to only the former having a native oxide, may account for the increase in conductivity in 50/51 but not in 50/52, for large negative gate bias.

Reduced Separation Between 2DEG and 2DHG

Figure 7.10 shows the drain characteristics of a device on wafer 50/53. This wafer differs from 50/51 (as presented in the structure shown in Figure 7.4) in that the thickness of silicon between the alloy layer and the oxide is only 30nm in 50/53, where in 50/51 it was 90nm. Figure 7.10 should be compared to Figure 7.6: quite a high current passes almost regardless of V_{GS} unless V_{DS} is less than half a volt where the modulation of the inversion layer varies the current.

This is not surprising if it is assumed that in 50/53 at room temperature, the shallow n^+ contacts reach close enough to the hole gas in the alloy layer to allow significant conduction at lower V_{DS} values than were needed to cause similar effects in 50/51.

Figure 7.11 shows this same effect more strikingly: in contrast to Figure 7.7, it is almost impossible to prevent current flowing between the shallow n^+ contacts unless a very small V_{DS} is applied.

Figure 7.10 Drain current characteristics of a gated Hall bar device on wafer 50/53, as measured using shallow n^+ contacts.

Figure 7.11 Transfer characteristics of a gated Hall bar on wafer 50/53, as measured using shallow n$^+$ contacts. The anomaly at V_{GS}=-100V is caused by the limited compliance of the gate voltage source and the capacitance of the device.

If it is possible to pass current between the shallow n^+ contacts via holes, it should be expected that it will be possible to pass current between the deep p^+ contacts via electrons and Figure 7.12 demonstrates this: for V_{DS} less than 1.5V, the current between the deep p^+ contacts is not influenced by the application of a *positive* gate bias. An inversion layer of electrons is forming at the silicon/silicon-dioxide interface but the resistance between the deep contacts is only visibly changed as V_{DS} increases past 1.5V.

The resistance between the deep p^+ contacts is decreased by positive gate bias, for large enough V_{DS}. Since it is unlikely at this temperature that depleting the hole population would lead to an increase in current flow then this effect must be caused by conduction through the electron inversion layer. This can be seen in Figure 7.13 (V_{DS} up to 1V) but not Figure 7.14 (V_{DS} up to 100mV): Figure 7.14 is similar in form to Figure 7.9 with roughly constant drain current at all positive gate bias values, but Figure 7.13 shows that drain current increases slightly as V_{GS} becomes more positive.

Room temperature measurement serves two purposes: firstly, it demonstrates the device as if it were a component in an everyday circuit (good performance in this context being the bottom line for efforts in silicon-germanium research) and also it demonstrates that it is worth performing characterization at low temperatures where device parameters can be extracted more easily.

7.4.2 2-terminal Characterization at Low Temperature

Contact Issues

Making reliable electrical contacts to semiconductor material has always been an issue. In the simplest case of metal on extrinsic non-degenerate silicon, there are two alternatives.

Figure 7.12 Drain current characteristics of a device on wafer 50/53, as measured using deep p^+ contacts under the influence of a *positive* gate bias.

Figure 7.13 Transfer characteristics of a gated Hall bar on wafer 50/53, as measured using deep p^+ contacts. The anomaly at V_{GS}=-100V is caused by the limited compliance of the gate voltage source and the capacitance of the device.

Figure 7.14 Transfer characteristics of a (different) gated Hall bar on wafer 50/53 as measured using deep p^+ contacts. Smaller V_{DS} has been applied in order to minimize conduction through the electron inversion layer, so that this figure can be compared in form with Figure 7.9.

If an n-type semiconductor is contacted with a metal and the work function of the metal is greater than of the semiconductor, or if a p-type semiconductor is contacted with a metal such that the work function of the metal is less than of the semiconductor, a depletion layer will form in the semiconductor at the junction, resulting in a rectifying Schottky contact.

However, if an n-type semiconductor is contacted with a metal and the work function of the metal is less than of the semiconductor, or if a p-type semiconductor is contacted with a metal such that the work function of the metal is greater than of the semiconductor, there will be no depletion layer and the contact will be Ohmic. Ohmic contacts are necessary for the passage of current of either polarity through a device, whilst Schottky barrier contacts are useful as gates for biasing purposes.

A device that features both n-type and p-type regions presents a problem as far as this approach goes, because different metals must be used for each type of contact if they are to have Ohmic characteristics. This problem is made worse if a significant density of semiconductor surface states are involved, since their effect is to generate a depletion layer at the junction by ‘pinning’ the Fermi surface in the middle of the band gap.

A way of avoiding this problem is to use very heavily doped contact regions, as these devices do. When a very heavily doped semiconductor is contacted with a metal, it may well form a Schottky contact. However, the heavy doping will result in the depletion layer being narrow enough that carriers can tunnel between the semiconductor and the metal to a useful degree.

To create such a heavily doped contact region, the semiconductor must be implanted with a high density of the relevant ions. This high density implantation causes damage to the crystalline structure of the semiconductor which spoils its electrical properties. In order to ‘activate’ the contacts and restore the crystalline nature of the heavily-doped contact region, the wafer must be annealed. In the case of the wafers under current discussion, the implants were activated with 30 minutes at

530ºC, in a nitrogen atmosphere. If the anneal is too long or hot dopants may significantly diffuse or the alloy layer may relax, but this step is insignificant compared to the native oxide growth, which required one hour at 720°C.

A contact created by implantation and annealing will not be truly Ohmic: the resistance of the contact will vary slightly with the voltage across the contact. However, this is not an issue if a 4-terminal method is used for measuring quantitative characteristics of the device provided that the resistance is never as high as, for example, the input impedance of the voltage measuring equipment (typically more than 10MΩ). However, it is possible that even if a contact is (approximately) Ohmic at room temperature, at temperatures lower than around 100K the contact will 'freeze out' and be useless. The IV curve of such a contact at 10K is shown in Figure 7.15. (This was a two-terminal measurement, and only one of the contacts used was frozen.)

For a Hall bar to be measurable, both of the current contacts and at least three out of the four voltage probe contacts must remain Ohmic. Unfortunately, it was found that only a small fraction of the contacts on each wafer remained Ohmic at low temperature. This is why no Hall mobilities will be presented for devices on wafer 50/53, and why many of the other structures fabricated on the wafers were not characterized.

Hysteresis

Figure 7.16 demonstrates how, as temperature decreases, hysteresis develops in the transconductance characteristics of the p-channel. When the gate voltage is increased the drain current decreases, and as temperature drops the drain current at positive gate voltages clearly saturates at lower and lower values. However, when the gate voltage is decreased there appears a peak in drain current. This hysteresis effect is present no matter how quickly the gate voltage is swept, but the high mobility peak does not persist for more than one hour at 10K if the gate voltage is held constant.

Figure 7.15 IV curve at 10K showing a deep, p^+ contact 'frozen out.' The resistance at 0V V_{DS} is almost 100MΩ, making the contact useless.

Figure 7.16 Temperature dependence of transconductance of a device on wafer 50/51 as measured using deep p^+ contacts, showing the development of the hysteresis. The drain voltage is 100mV.

Figure 7.17 shows transconductance characteristics of the n- and p-channels of a (different) device on wafer 50/51 at 10K. Hysteresis is visible in the n-channel but is not as striking as in the p-channel. Also, the conductance of the n-channel is generally inferior to the p-channel. Hopefully, Hall effect measurements (section 7.5) will help begin to explain the hysteresis phenomenon.

Conduction Between Deep and Shallow Contacts

It would be fascinating to compare these results with similar results for a device with a much smaller separation between the electron and hole systems. However, no devices existed on wafer 50/53 which had a sufficient number of Ohmic contacts at 10K, so systematic studies and Hall effect measurements (as will be presented in the following section) were out of the question.

However, Figure 7.18 shows how the vertical field within the device can induce a small current between the deep and shallow contacts: with the drain connected to the deep p^+ contacts and the source connected to the shallow n^+ contacts, V_{DS} was held at 0V whilst V_{GS} was swept. The bending of the bands in response to the gate potential induces a small current between the deep and shallow contacts. A feature can be seen at +20V which corresponds to the formation of the electron inversion layer. A similar spike was seen at V_{GS}=40V when measuring a device on wafer 50/51 in the same way. As the gate voltage is decreased from 100V to 0V, a dip can be seen is this area. A small spike can be seen at around -15V as V_{GS} is decreased further, which may correspond to the formation of a hole gas at the oxide interface. The data is discontinuous at 0V due to hysteresis.

Figure 7.17 The transconductance characteristics of the n- and p-channels of a device on wafer 50/51 at 10K, showing hysteresis. The drain voltage is 100mV, the n-channel threshold voltage is around 30V, greater if the gate voltage is decreasing rather than increasing.

Figure 7.18 With the drain connected to the deep p^+ contacts and the source connected to the shallow n^+ contacts, V_{DS} was held at 0V whilst V_{GS} was swept. The bending of the bands in response to the gate potential induces a small current between the deep and shallow contacts. A feature can be seen at +20V which corresponds to the formation of the electron inversion layer.

The IV characteristics of such a "tunnelling" arrangement (with current passing vertically through the device between deep and shallow contacts) are interesting but inconclusive. It is clear, though, that there is more to the behaviour than the interaction of the shallow contacts themselves and the hole gas in the alloy layer because there is a dependency on the gate bias, and therefore the electron density in the inversion layer. Such behaviour is probably worthy of detailed study at very low temperatures, in a device with a full set of Ohmic contacts.

7.5 Hall Effect Results

Data in this section was mainly obtained using a d.c. method employing the HP parameter analyzer (described in section 4.2.1) and a differential amplifier developed by R. J. P. Lander (although some results were previously obtained using an a.c. lock-in amplifier method). This meant that potentials between contacts of 0.1µV could be resolved, increasing the sensitivity by a factor of 1000 over the HP alone.

The Hall effect shows that the system enters a high resistivity phase at a Hall sheet density (Equation 4.7) of 8×10^{11}cm^{-2}. This is seen as the gate voltage increases past -10V, and also as the gate voltage decreases past 70V. The Hall effect calculation ceases to be applicable: it yields zero mobility and undefined sheet density indicating non-metallic, 'hopping' transport.[26,27] These points have been removed from Figure 7.19 for the sake of clarity. This could be interpreted as a metal-insulator transition; the longitudinal resistivity at this transition is roughly ${}^{h}\!\big/_{2e^2}$.

Figure 7.19 Single carrier Hall calculations (from Chapter 4) applied to ρ_{XX} and ρ_{XY} data from the deep p^+ contacts of a Hall bar device on wafer 50/51 at 10K. The solid line is data taken as the gate voltage decreases from +100V to -100V, the dotted line is data taken as the gate voltage increases. This should be compared with the low temperature data in Figure 7.16.

Figure 7.19 shows fairly conventional behaviour for gate voltages in the range -100V to -10V. Sheet density increases as the gate voltage is made more negative, and the mobility correspondingly decreases. (Mobility versus sheet density is shown in Figure 7.20). However, in the gate bias region between -10V and +100V the density and mobility are subject to the same hysteresis as the transconductance: in fact, there is a mobility peak at the (decreasing) V_{GS} of 25V of 2,100cm^{2}V^{-1}s^{-1} (corresponding to a sheet density of 1×10^{12}cm^{-2}; a similar sheet density is seen at a V_{GS} of -25V, but here the mobility is only 1,500cm^{2}V^{-1}s^{-1}) which suggests that the conducting channels are of different natures. This suggests that single-carrier Hall calculations will be misleading. In fact, since the heterostructure was designed to produce a 2DHG with a sheet density of 3×10^{11}cm^{-2}, and consideration of the discussion in Chapter 3 suggests that a sheet density as high as that measured in the alloy layer is physically impossible, either the Hall scattering factor is less than unity even at 10K, additional conduction channels are present, or the structure itself deviates from specifications.

As Chapters 4 and 6 make clear, this is the sort of problem that magnetoresistance and mobility spectrum analysis would be well-equipped to address. However, in this case there is the additional complication that the state of interest (induced by bringing the gate voltage down from 100V to 25V) decays significantly in the time taken to acquire magnetoresistance data. A solution, involving a gate bias which is cycled between 100V and 25V for every measurement (of which there are typically 512 or 1024) would add considerably to the time and complexity of the experimental procedure.

Interpretations of Hall Effect Results

As Figure 7.16 shows, at large positive gate biases (particularly for the case where the gate voltage is increasing) the conductivity through the device drops with temperature. This, along with the disappearance of the Hall effect mentioned above, is consistent with the behaviour of conduction through boron-doped silicon in which transport is freezing out.[27]

Figure 7.20 The same data as in Figure 7.19 but plotted as (Hall) mobility against sheet density. The data representing decreasing gate voltage (leftward-pointing triangles, solid line) stand out as a high mobility peak at a sheet densities just over 1×$10^{12}$$\mathrm{cm}^{-2}$.

At the negative bias limit, it assumed that hole gases exist both within the alloy and at the oxide interface, as is usual in gated heterostructures.[28] If free charge exists within the cap layer, the gate and the alloy layer are screened from each other.

Simulations of the band profile which solve the Poisson equation in one dimension (or even solve the Poisson and Schrödinger equations self-consistently) are not strictly applicable to this hysteresis effect at low temperatures, since it is evidence of a system out of equilibrium. Some results of simulation at higher temperatures will be presented in the following section.

Possible Causes of Hysteresis

Hysteresis effects are seen in MOS systems where traps exist in, or ions are moving through, the gate oxide in response to the gate bias.[11,29] Consider that mobile positive ions (for example, Na^+) exist in the oxide of a device with a certain threshold voltage for electrons. Upon application of a strong positive gate bias, these charges will be forced away from the gate, towards the oxide interface. If the positive charges remain at the interface when the bias is removed then effectively a fraction of the positive bias is stored at the interface. Therefore, a slightly more negative voltage is now required (compared to before the charge was moved by the strong bias) to counteract this stored charge. The threshold voltage for inversion is therefore moved to a more negative gate bias due to the application of a strong positive bias. This is the *opposite* of the observed behaviour in Figure 7.17, so cannot be the correct explanation.

The hysteresis in Figure 7.17 is also in the opposite sense to that seen in n-channel silicon-on-insulator MOS transistors.[30] Hysteresis has been observed in the I_D versus V_{DS} behaviour of silicon MOS transistors at 4.2K[31,32] where it is discussed in terms of self-heating (not thought to be important and not relevant in this system where the hysteresis is in the I_D versus V_{GS} behaviour) and field-induced dopant ionization.[33]

The fact that the hysteresis effect grows in significance on the same temperature scale that transport in the boron doping slab freezes out (around 60K, related to the energy of the acceptor level in boron) would suggest that ionization of the dopants induced by changes in bias conditions may be relevant. The transients seen in Figure 7.18 which show charge moving vertically through the device back this up.

7.6 Analysis

Carrier Gas Formation

Simulations were performed using the FISH1d software package, running on the public-access Purdue University Network Computing Hub, PUNCH. This software numerically solves the one-dimensional equilibrium Poisson equation in a semiconductor heterostructure at a given temperature, under specified bias conditions.[34,35]

Figure 7.21, featuring results from simulating the structure of wafer 50/51 at 300K, shows that the electron gas at the oxide interface does not co-exist with a hole gas in the alloy of roughly equal density at any gate bias, and therefore that the band profile in Figure 7.1 is never realized in this heterostructure: the band profile is closer to the lower panel of Figure 7.3. The x-axis scale is arbitrary since the thickness of the oxide and the possibility of interface charge is ignored. (The positions of the electron and hole thresholds, which can be compared to Figure 7.7 and Figure 7.9 respectively, suggests that experimental zero bias corresponds to a simulation bias of around -0.3V.)

The density of free holes in the dopant layer, not shown in Figure 7.21, varies from $4.7\times10^{12}\text{cm}^{-2}$ at the most negative bias to $4.6\times10^{12}\text{cm}^{-2}$ at the most positive. Since the Fermi level is pinned close to the valence band by the dopant, a small number of carriers are present in the region un-doped silicon spacer layer.

Figure 7.21 should be compared with Figure 7.9: drain current varies very little for gate voltages larger than 20V, since current flow is almost entirely through the dopant layer.

Figure 7.21 Results of simulations of 50/51 which solve the one-dimensional Poisson equation. The temperature is 300K. The x-axis scale is arbitrary, since it does not take into account the oxide thickness or interface charge. The two important features are that the electron and hole gases never coexist, and that the density of holes in the alloy reaches a relatively small value before the cap layer begins to populate.

The slight increase in current flow as V_{GS} decreases from 20V to -5V corresponds to the region in Figure 7.21 where the population of holes in the alloy and spacer layer is increasing; the large increase in current flow from -5V to -100V corresponds to the formation of a hole gas at the oxide interface. This means that most of the variation in conductance between p-type contacts is due to the gate bias modulating the density of a hole gas formed at the oxide interface.

Figure 7.22 shows results of simulations of wafer 50/51 at 77K: the gate bias does not go negative enough to induce a hole gas at the oxide interface, and the problem of the electron and holes gases not co-existing is worse than at room temperature.

Simulations of wafer 50/53 at 300K are shown in Figure 7.23. The thin cap (30nm rather than 90nm as in 50/51 or 50/52) essentially increases the capacitance of the device (increases the number of holes in the cap layer) but does not change the fact that significant numbers of electrons and holes never co-exist.

Issues with the Original Design

The above results of simulation make it clear that Figure 7.1 is inaccurate; in fact, it is fundamentally unphysical. In one dimension, Poisson's equation can be written as

$$\frac{d^2V}{dz^2}=\frac{-en(z)}{\epsilon_r\epsilon_0} \qquad 7.2$$

where $n(z)$ represents the number density of free charges at a depth z within a semiconductor of relative permittivity ε_r.[11,12] Integration of Equation 7.2 with a constant n leads to:

$$V(z)=-\frac{en}{2\epsilon_r\epsilon_0}z^2+Az+B \qquad 7.3$$

Figure 7.22 Results of simulations of 50/51 similar to Figure 7.21 but with a temperature of 77K. Again, the electron and hole gases never coexist.

Figure 7.23 Results of simulations of 50/53 which solve the one-dimensional Poisson equation. The temperature is 300K. The alloy population reaches a slightly larger value than in Figure 7.21 before the cap layer begins to populate, but otherwise the important features are the same.

The constants *A* and *B* describe, respectively, the external electric field and the external potential. If the system is treated as closed, with only changes in potential through the device being relevant, then only the first term in Equation 7.3 is important.

The implications of Equation 7.3 are that the gradient of the bands (that is, the electric field) within a semiconductor changes where, and only where, free charges are present. Further, the gradient of the bands is proportional to the difference between the total amount of free charge to be found in either direction. It is assumed that the background (unintentional) impurity level within typical heterostructures is at most 10^{15}cm^{-3}, four orders of magnitude lower than the level of intentional doping,[21,25] so the scale on which ionization of unintentional dopants leads to significantly curved energy bands is at least 100 times longer than the scale on which the energy bands curve in regions of ionized intentional doping or the width of the wavefunction of a 2-dimensional carrier gas, which is the order of 10nm.[12,25,36]

This band bending can be seen in Figure 3.1: the gradient of the bands changes only where ionized dopant or the carrier gas itself exists. In the setback region, the presence of ionized dopant atoms (negative free charges) below and the carrier gas (positive free charges) above results in an electric field, and therefore a sloping energy band. Since the carrier gas and ionized dopant densities exactly cancel, there is no electric field above the alloy layer and so the bands are flat.

Thus Figure 7.1, reproduced exactly from Reference 21, is misleading since the slope of the energy bands implies that the electric field between the 2DEG and the 2DHG is exactly the same as the field between the 2DHG and the dopant layer. This is only possible if the 2DHG density is actually zero.

There are examples in the literature of hand-drawn band profiles used to justify and illustrate heterostructure designs[13,14,16] which clearly violate Poisson's equation. In some cases, it is possible that a proper consideration of the band profile would show the structure to be of little use for its intended purpose. Whilst a full Poisson-Schrödinger solution is overkill when a device is being sketched out within a proposal or review, it is hoped that consideration of the following discussions of device design will lead to a greater intuitive sense of the band profile in a semiconductor heterostructure.

Calculation of the Expected Sheet Density

The following is assumed to be valid for "zero" temperature, which in this context means that $T \ll T_F$ where T_F is given by Equation 3.5. The effective mass m^* is taken to be $0.3m_e$ (based on the results in Chapter 5) giving a T_F of 30K (from Equation 3.5) if the simple calculation given in Equation 7.1 is assumed to be valid.

Firstly it is assumed that the Fermi level is pinned in the bulk of the Boron doping slab, at a level of E_A~30meV relative to the band edge, and that the width of the depletion region at the edge of the doped region is much less than the setback d, which is reasonable considering the high Boron concentration. It is then assumed that the confining potential in the alloy is triangular, with energy levels:[25]

$$E_n = \left(\frac{\hbar^2}{2m*}\right)^{1/3} \left(\frac{3}{2}\pi q F_0\right)^{2/3} \left(n+\frac{3}{4}\right)^{2/3} \quad (n=0,1,2...) \qquad 7.4$$

where $$F_0 = \frac{p_S q}{\epsilon_0 \epsilon_{Si}} \qquad 7.5$$

Only the n=0 level is significantly occupied when $T \ll T_F$ so the picture in Figure 3.2, which shows the Fermi level at $\frac{\hbar^2 k_F^2}{2m^*}$ from the E_0 subband, holds. E_0 calculated with the sheet density value obtained from Equation 7.1 is 32meV, and the Fermi energy E_F from Equation 3.5 is 2meV. Equation 7.1 can now be modified to take these into account, assuming flat bands everywhere else in the structure and that the dopant depletion region is narrow:[25]

$$\frac{p_S q}{\epsilon_0 \epsilon_{Si}} = \frac{\Delta E_V - E_0 - E_A - E_F}{d} \qquad 7.6$$

The sheet density consistent with this field in the setback is 1.4×10^{11}cm^{-2}, around half that of the value found from Equation 7.1. Further iteration around the system of Equations 3.5, 7.4, 7.5 and 7.6 leads to convergence on a sheet density of 1.7×10^{11}cm^{-2}. This analysis ignores background doping of the supposedly intrinsic layers of the structure and charged interface impurities.* Typical values for these parameters are of the order of magnitude of the calculated sheet density but essentially unpredictable, so their incorporation into Equation 7.5 (see Equation 3.1) would introduce a significant degree of arbitrariness.[25]

However, as made clear by Figures 7.21, 7.22 and 7.23, any application of positive gate bias in order to form an inversion layer of electrons will first deplete the hole gas in the alloy layer, leading to a band profile similar to Figure 7.3. The designed-in hole gas density must be much greater than that which is intended to be present when the electron gas is formed, if they are to co-exist.

7.7 Specifications For New Structures

7.7.1 Vertically Integrated MOSFET

It is generally true that for hetero-MOSFETs to operate usefully, the cap layer must be thin enough that the gate bias modulates the hole density in the alloy layer without forming an inversion layer at the oxide interface.[28] Figures 7.21 and 7.23 show that this is not the case when the cap layer is 90nm or even 30nm thick. In fact, cap thicknesses of less than 10nm are under consideration for current HMOS research devices.[37]

Devices on 50/53 showed serious leakage between the shallow (25nm) n$^+$

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* It is possible that a setback of 34nm was chosen to allow for segregation of boron dopant atoms. This would mean that the true setback would be much smaller. However, to achieve a carrier concentration in the alloy of 10^{12}cm^{-2}, the setback would need to be less than 5nm.

contacts and the alloy channel (at a depth of 30nm) so in a thin-cap structure, the n^+ contacts must be very shallow indeed.

Another issue with these devices is that, at room temperature, there is always conduction between the deep p^+ contacts through the boron doping layer. This doping layer is important to ensure that a hole gas forms in the alloy layer under the application of negative gate bias, well before the oxide interface becomes significantly populated with holes, although this may be accomplished by much weaker doping than is used here. However, if the deep contact implantation is performed at such an energy that the alloy is contacted but the boron doping slab is not, then the depletion region in the setback should ensure that conduction is only possible through the hole gas in the alloy layer.

7.7.2 Co-existing Electron-Hole Gas Systems

The calculation presented above can be adapted to consider co-existing electron and hole gases. A proposed band profile is shown in Figure 7.24 which can be compared to Figure 7.1. Assuming that a consistent solution exists, that background doping ionization and interface impurities are negligible, and that the dopant depletion width is small (since the dopant dose is very high) the electric field in the setback between the dopant layer and the alloy is:

$$F_d = \frac{(p_M - n_S + p_S + n_A^-)q}{2\epsilon_r\epsilon_0} = \frac{n_A^- q}{\epsilon_r\epsilon_0} \qquad 7.7$$

where n_A^- is the sheet density of ionized dopant atoms, n_S is the electron carrier concentration in the 2DEG, p_S is the hole carrier concentration in the 2DHG and p_M is the concentration of positive charges on the metal gate. The electric field in the cap layer is:

Figure 7.24 Proposed (low temperature) band profile of a device which will feature co-existing electron and hole 2-dimensional gases.

$$F_s = \frac{(p_M - n_S - p_S + n_A^-)q}{2\epsilon_r\epsilon_0} = \frac{(n_A^- - p_S)q}{\epsilon_r\epsilon_0} \tag{7.8}$$

Equations 7.7 and 7.8 explain that the presence of these charges create sloping bands, and make use of overall charge neutrality: $p_M = n_S - p_S + n_A^-$. However, in order for the charges to be present, the fields must be such that the bands cross the Fermi level as shown in Figure 7.24 and this condition can be summarized such that

$$qF_d d = -E_A + \Delta E_V - E_F^+ - E_0^+ \tag{7.9}$$

$$qF_s(s+t) = E_G - \Delta E_V + E_F^+ + E_0^+ + E_F^- + E_0^- \tag{7.10}$$

where E_A is the acceptor level in the dopant layer, E_G is the silicon band gap, ΔE_V is the valence band offset, E_F^+ is the Fermi level and E_0^+ is the subband ground state energy for holes in the 2DHG (see Equations 3.5 and 7.4, and Figure 3.2) and E_F^- and E_0^- are the corresponding quantities for the 2DEG. The relative permittivity of germanium is higher than that of silicon, but in considering a thin layer of an alloy with a low germanium content this is ignored.

From charge neutrality it can be seen that if $n_S = p_S$ then $p_M = n_A^-$. Substitution of Equations 7.7 and 7.8 into 7.9 and 7.10 gives:

$$p_S = n_S = \frac{\epsilon_0\epsilon_r}{q^2}\left[\frac{1}{d}(-E_A + \Delta E_V - E_F^+ - E_0^+) - \frac{1}{s+t}(E_G - \Delta E_V + E_F^+ + E_0^+ + E_F^- + E_0^-)\right] \tag{7.11}$$

If the two largest energies in Equation 7.11 are ΔE_V and E_G (for a 20% germanium alloy $\Delta E_V = 140meV$ whereas $E_A \sim E_0 \sim 30meV$ and $E_F \sim 3meV$)[23] then

$$p_S = n_S \simeq \frac{\epsilon_0 \epsilon_r}{q^2} \left[\frac{\Delta E_V}{d} - \frac{E_G - \Delta E_V}{s+t} \right] \qquad 7.12$$

A setback d of 34nm and a gas separation $s+t$ of 105nm leads to an unphysical negative result for p_S and n_S. For a positive solution to Equation 7.12 to exist in a 20% germanium alloy system, the spacing between the gases must be more than 7 times the setback. If the setback were 10nm, carrier gases may co-exist according to this approximation. However, once the zero-point energy of each triangular quantum well is taken into account, it becomes non-trivial to find a solution. A self-consistent solution may not exist at all unless very germanium-rich alloys (which are hard to grow pseudomorphically)[20] are used. For a fully-strained pure germanium channel on pure silicon, with a 10nm setback and 100nm between carrier gases, Equation 7.12 suggests coexisting gases, each with a density of more than 4×10^{12}cm^{-2}.

From the starting points described above, a true Poisson-Schrödinger solution method may be used to find the electron and hole gas sheet densities. However, it is not guaranteed that there will be a solution featuring matched and coupled-channels for a given carrier gas spacing or hetero-offset, even if Equation 7.12 is fulfilled; the device specifications themselves must be part of the iterative process. A method of genetic algorithms may be suited to finding a viable device structure.

It is also possible that more exotic structures (involving n and p-type modulation doping, a virtual substrate or a strained-silicon electron channel) would lead to co-existing electron and hole gases which are closer together and each have a high enough sheet density to be metallic.

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